REMARKS

Remaining Claims

Forty-one (41) claims (Claims 1 - 41) remain pending in this application through this Amendment. Claims 1, 10, 28, 37, and 40 have been amended by this amendment.

Allowable Subject Matter

The Applicant wishes to thank the Examiner for recognizing the allowable subject matter of allowed claims 19 – 27 and 33 – 36 and of objected-to claims 7-9, 11-13, 15-18, and 29-31, which depend directly or indirectly from the allowed claims.

Rejection of Claims 1, 2, and 37 under 35 USC §102(e) – Jinbo et al.

Claims 1, 2, and 37 are rejected under 35 USC §102(e) as being anticipated by Jinbo et al. (U.S. Patent No. 6,438,081). The Applicant respectfully traverses the rejection.

Claim 1, as originally filed, recites "each sampler sampling ***a transition and data*** of the input data signal" (Emphasis added). In accordance with the invention, each sampler samples both a transition and data of the incoming data signal. By using multiple samplers, each of which samples a transition and data, the samples can be combined to obtain two adjacent data, or bit, samples and an intermediate transition sample. These two adjacent bit samples and the intermediate data sample are then logically combined in a known manner using an early-late ATB detector to obtain early-late error indications. (See Fig. 1 and page 8, lines 5 – 19 of the present application).

Neither Jinbo et al. nor any of the other prior art of record teach or suggest a multi-phase sampling system that uses multiple samplers, each of which samples both a transition and data of an incoming signal, as recited in independent claim 1. The Examiner states that Jinbo et al. discloses "each sampler sampling a transition of the input signal and outputting a respective output". The Examiner does not contend that Jinbo et al. discloses sampling a transition of the input signal *and data*, as recited in independent claim 1 of the present application. It appears that the Examiner may have overlooked this feature of the invention. To further clarify this feature of the invention,

independent claims 1, 10, 28, 37, and 40 have been amended to state that each sampler samples a portion of the input data signal corresponding to a transition of the input data signal and a portion of the input data signal corresponding to data.

For example, independent claim 1 has been amended to state:

"each sampler sampling a portion of the input data signal corresponding to a transition ~~and data~~ of the input data signal and a portion of the input data signal corresponding to data, the portion of the input data signal corresponding to data being in between two consecutive transitions of the input data signal, each sampler outputting a respective output signal."

Independent claims 10 and 28 have been amended to state that each of the first, second and third sampling devices samples "the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal".

Independent claims 37 and 40 have been amended to state:

"each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal".

Jinbo et al. does not teach or suggest that each latch samples the binary signal at a portion of the binary signal corresponding to a transition and at a portion of the binary signal corresponding to data. The Examiner refers to Figs. 2 and 7 and Col. 7, lines 52-59 in Jinbo et al. The goal in Jinbo et al. is to ensure that the timing of the sync clock signal 14 relative to the timing of the binary signal 11 is such that the rising edge of the sync clock signal 14 does not occur when a level change is occurring in the binary signal 11. This, in turn, ensures that the latch FFc (Fig. 7) that samples the binary signal 11 and that is triggered by the sync clock signal 13 will sample the binary signal 11 at a time other than during a level change of the binary signal 11.

To accomplish this, Jinbo et al discloses using five latches FFa – FFe to sample the delayed binary signal 11 and the outputs of the latches are input to a phase

discrimination circuit 40, which determines where the phase change in the delayed binary signal occurred. Based on this determination, the binary signal 11 is delayed so that the point in the delayed binary signal 24 where the level change is occurring is moved in time away from the point in time at which the rising edge of the sync clock signal 14 is occurring. This ensures that latch FFc will sample the delayed binary signal 24 at a point other than during a transition of the delayed binary signal 24. The output of latch FFc corresponds to the reproduced binary signal 15.

None of the latches FFa – FFe sample both a level change (i.e., a transition) of the delayed binary signal 24 and data. Each of the latches samples only one point of the delayed binary signal 24 to provide the phase discriminating circuit 40 with enough data samples for it to judge the time relationship between the delayed binary signal 24 and the multi-phase clock signals CLK1 – CLK5. Jinbo et al. states:

> The judgement of the time relationship between the phases of the multi-phase clock signals CLK1 to CLK5 and the phase of the binary delayed signal 24, is required to wait until the latch data of all the latch circuits FFa to FFe are updated or provided in a duration corresponding to at least one period of the sync clock signal 14.

Thus, it is clear that none of the latches obtain more than one sample of the delayed binary signal. Furthermore, the latch FFc that samples the delayed binary signal 24 and outputs the reproduced data signal 15 never samples a transition. The goal of the invention described in Jinbo et al. is to ensure that latch FFc always samples the delayed binary signal 24 at a point in time other than during a transition.

In order for a claim to be anticipated under 35 U.S.C. §102, all of the elements in the claim must be disclosed in a single reference. For at least the reason that Jinbo et al. does not disclose each sampler sampling a transition and data, as recited in each of the independent claims of the present application, the Applicant respectfully submits that none of the claims of the present application are anticipated by Jinbo et al. Accordingly, the Applicant respectfully requests that this rejection be withdrawn.

Rejection of Claims 3, 4, 38, and 39 under 35 USC §103(a) – Jinbo et al. in view of LaRosa et al.

Claims 3, 4, 38, and 39 are rejected under 35 USC §103(a) as being unpatentable over Jinbo et al. (U.S. Patent No. 6,438,081) in view of LaRosa et al. (U.S. Patent No. 5,247,544). The Applicant respectfully traverses the rejection.

For at least the reason that claims 3, 4, 38 and 39 depend either directly or indirectly from either of independent claims 1 or 37, which are believed to be allowable for the reasons stated above, claims 3, 4, 38 and 39 are also believed to be allowable over Jinbo et al. in view of LaRosa et al.

Furthermore, LaRosa et al. also does not teach or suggest each sampler sampling both a transition and data. Each of the sample-and-hold circuits 303, 305, 307 and 309 obtains exactly one sample at a particular point in time. The four samples are then processed to produce four respective error signals 347, 349, 351, and 353. The sampling phase adjustment circuit 327 then advances or retards the four clock signals 339, 341, 343, and 345 that trigger the four sample-and-hold circuits 303, 305, 307, and 309 accordingly. There is no reason for each sample-and-hold circuit to sample both a transition and data, and LaRosa does not teach or suggest doing so.

Rejection of Claims 5 and 6 under 35 USC §103(a) – Jinbo et al.

Claims 5 and 6 are rejected under 35 USC §103(a) as being unpatentable over Jinbo et al. (U.S. Patent No. 6,438,081). For at least the reason that claims 5 and 6 depend from independent claim 1, which the Applicant believes is allowable over the prior art of record for the reasons set forth above with reference to the rejection of claims 1, 2 and 37, the Applicant respectfully submits that claims 5 and 6 are also allowable over the prior art of record. Accordingly, the Applicants respectfully requests that this rejection be withdrawn.

Rejection of Claims 10, 14, 28, 32, 40 and 41 under 35 USC §103(a) – Jinbo et al. in view of LaRosa et al.

Claims 10, 14, 28, 32, 40 and 41 are rejected under 35 USC §103(a) as being unpatentable over Jinbo et al. (U.S. Patent No. 6,438,081) in view of LaRosa et al. (U.S. Patent No. 5,247,544). The Applicant respectfully traverses the rejection.

As stated above, claims 10 and 28 both recite that each of the first, second and third sampling devices samples "the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal". Claim 40 recites: "each of the sampling devices sampling the first data signal at a portion of the first data signal corresponding to a transition of the first data signal and at a portion of the first data signal corresponding to data, the portion of the first data signal corresponding to data being in between two consecutive transitions of the first data signal". Claims 14, 32 and 41 depend directly or indirectly from claim 10, claim 28 or claim 40.

As stated above, neither Jinbo et al. nor LaRosa_et al. teach or suggest the above-quoted features of the invention. For at least this reason, the Applicant respectfully submits that claims 10, 14, 28, 32, 40 and 41 are patentable over Jinbo et al. in view of LaRosa et al., and the Applicant respectfully requests that this rejection be withdrawn.

CONCLUSION

For the reasons set forth above, it is respectfully submitted that all pending claims are now in condition for allowance, and Applicant requests a Notice of Allowance be issued in this case. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
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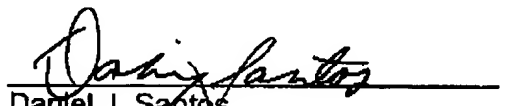

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